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LCD Resources:

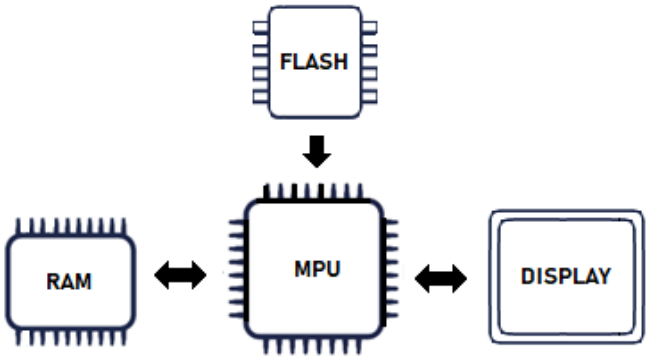
MIPI DSI Display Memory

MIPI DSI Display Memory

MIPI DSI is an interface that can provide dynamic graphics and high resolutions. Maximum color depths at fast communication speeds are accessible over differential data lines to render images and videos to the display. MIPI DSI displays have become a popular choice because they support high quality graphics with fewer pin connections.

Large amounts of pixel data are used to create the colorful and defined images. The data is stored in a memory location called the frame buffer. The frame buffer must be provided by the display or by the processor. The MIPI DSI interface offers an alternative by operating the display in video mode.

This resource will discuss the options for storing large amounts of image data and the operating modes available in the MIPI DSI communication protocol. There are two modes available when memory is accessible to the display. The modes are differentiated by the location of frame buffer provided for display data. The substitute for display memory is to operate the display in video mode which does not require memory access. Considerations of memory location and access should be made when using the MIPI DSI protocol.



High resolution displays have a larger number of pixels and require more memory. An increased color depth means there is more data assigned to each pixel. For true color (RGB-888) each pixel is assigned 24-bits of color. This data needs to be stored in a location accessible by the microprocessor and the display. The minimum memory requirement for the framebuffer is calculated by the following equation.

Frame Buffer Memory = Resolution x Color Depth

For example, a display with a 480x800 pixel resolution operating in true color (24bpp) would have a minimum framebuffer requirement of:

480 pixels x 800 pixels x 24 bits/pixel = 9.2M-bits or 1.15M bytes

This is the memory for one full frame of image data. There are options for efficiently storing display data and maximizing available memory. A lower color resolution can be set with minimal reduction or visible effect on the image. Partial image storing is another way to conserve memory. The frame buffer will contain a portion of the frame that is to be updated. This can be referred to as layering and only certain layers are refreshed.

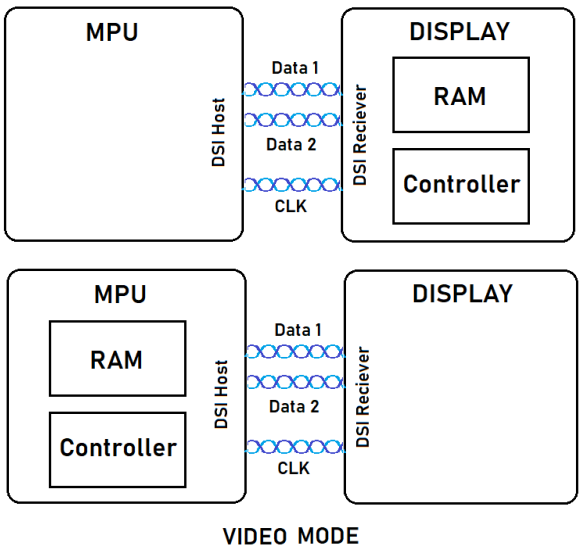
The location of the frame buffer memory is dependent on what is available and what can be accessed at a speed compliant with the MIPI DSI interface. The MIPI DSI display interface requires high speed memory access to prevent flickering and tearing on the display. Each location of memory has its own benefits and constraints. The display memory can be stored in the following locations for the MIPI DSI interface.

- Internal Display RAM
- Internal MPU RAM
- External RAM or Controller

The MIPI DSI protocol communicates at high speeds of up to 1Gb/s for 2-data lane interfaces. The location of RAM will need to be accessed by the MPU and forwarded to the display at a speed fast enough to meet minimum interface requirements.

The method of DSI communication is determined by the location of memory. This can include how the data is formatted, the required speed of communication and the DSI mode used. The DSI protocol offers two communication modes: command and video. This determines how data will be sent and where it is stored.

The two DSI communication modes are portrayed below. Each mode has RAM and the controller in a different location.



VIDEO MODE

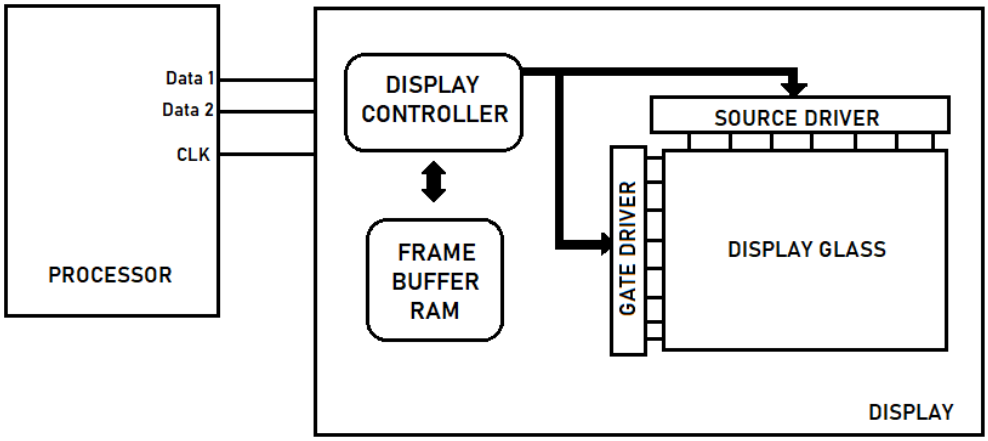
The display memory is customizable by location, amount available and the desired display application. Pixel data can be stored in partial frames to conserve memory. The images can be programmed in independent layers to minimize the amount of data that needs to be refreshed. The layers can be stored in different memory locations on the processor which provide more accessible memory for image data.

RAM can also be provided external to the display and microprocessor. External RAM can provide more memory than internal memory systems, but considerations should be made for access and operational timings.

Display IC Internal RAM

The MIPI DSI displays have an embedded controller IC that can be used to format pixel data. The display IC's come in versions with and without display data RAM (DDRAM). Display modules without internal RAM are lower in price and more common in DSI displays. The memory will have to be provided externally or different methods of operation can be implemented.

The frame buffer can be stored in the internal display RAM and accessed by the display controller IC. The image data is written to display RAM by the controller through specified commands. Other commands are used to specify color format, voltage settings and data types. In this scenario, the display does all of the heavy lifting. This frees up the microprocessor for other processes and the display can operate while the MPU is idle.



Another benefit of using internal display RAM is that the physical memory addresses correspond to the pixel display area. In other words, the frame buffer is the same size as the resolution. The internal display RAM provides the exact amount of memory for the display resolution. This makes reading and writing to RAM simple. Display RAM typically provides enough memory for one full page of image data at high color. This can often be more than what is provided on the MPU.

The MIPI DSI protocol has two operation modes. The command mode is used when the display has access to the internal frame buffer memory. The display controller receives commands from the processor and then formats the data to store in the frame buffer for the next display refresh.

The display is operated by specified commands that will address the memory of the frame buffer internally. The commands are sent over a low power and short packet data type. These commands will initialize the driver to handle the data. The data can be sent in long packets at high speeds to be stored in internal memory and accessed for the next fresh cycle.

MIPI DSI displays that contain internal RAM can operate in command and adapted command modes where display data sent to and controlled internally. This reduces the CPU required from the microprocessor because the display handles the memory and image processing. This reduces the potential bandwidth limitations on the MPU.

MPU Internal RAM

The microprocessor interfaced with the display can provide the memory for display data. This method is used when there is not memory provided internally by the display. Storing the data internally in the processor provides efficient access to display data that can be quickly sent to the display. Using memory internal to the processor is the fastest method for transmitting data. The MPU can read from and write to internal RAM and communicate it to the display through the DSI at high speeds.

Internal RAM is a limited resource for many processors. Most processors will not have the memory available for a full page of display data especially at high resolutions and high color formats. Steps can be made to maximize available MPU memory usage. Display data can be stored in layers that make up portions of the full frame. Updating smaller portions of the display can conserve memory instead of storing and continuously updating the full frame.

Storing data in partial frame buffers reduces the amount of memory stored in RAM but requires more drawing operations to be performed between the display and the processor. The means that more transfers to the display are needed and thus a faster interface clock is required.

A lower color format can be chosen without a significant reduction to image quality . The color format of the frame buffer determines how much memory is required for the page. The memory required for the frame buffer of a 400x800 pixel display with 24bpp color depth is 1.5MB. At 16bpp, RGB-565, the memory required for the same resolution is reduced to 768kB. Different layers and partial frames can be programmed to have independent color formats.

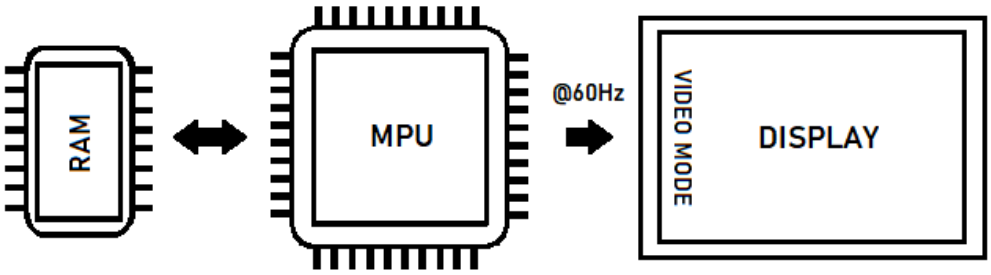
Color Formats to Memory Requirements

Resolution	Bits per Pixel	RGB Format	Memory Bits	Memory Bytes
480 x 800	24	8, 8, 8	9.2Mbits	1.15MB
	18	6, 6, 6	6.9Mb	864kB
	16	5, 6, 5	6.14Mb	768kB
400 x 640	24	8, 8, 8		
	18	6, 6, 6	4.6Mb	576kB
	16	5, 6, 5	4.09Mb	512kB

Video Mode and Internal RAM

The MIPI DSI protocol offers two modes: command and video. The video mode is used when the display does not have access to internal RAM. The video mode sends the data from the processor to the display in a continuous stream. The MPU is required to stream the data which increases the bandwidth of the system processor.

In video mode, the processor sends the packets of display data through the high speed MIPI DSI link. The high-speed data is transmitted in long packets structured by synchronization signals to specify horizontal and vertical timings. The display data is streamed in this sequence at a continuous refresh rate.



The video mode of the MIPI DSI protocol relies on internal RAM to be provided by the host processor. It is used when the display does not provide internal display RAM or if the display does not have an internal controller. The synchronization event can be sent in brief low power operation events or as null data events. These events also structure the begin and end of a DSI data packet.

Video mode places more demand on the host processor. The processor is continuously streaming the pixel data which requires a higher bandwidth. Synchronization timing events need to be calculated and implemented into the high-speed packets of display data to properly frame the image.

The video mode of the MIPI DSI communication protocol consumes more power than the low power command mode. The high-speed video mode can incorporate low power transition times between lines or frames to conserve power while synchronizing the display data. The low power modes indicate the begin and end flags of packet data.

External RAM

In cases where internal RAM is not used, external RAM can be incorporated into the system. External RAM provides more memory than the internal systems. Storing the frame buffer in external memory can be slower to access than to internal memory. The processor will have to access the external RAM and forward the information to the display at a speed fast enough to maintain the minimum frame rate requirements.

Using external RAM allows for multiple buffers to be incorporated into the system. Since there is enough memory available, multiple buffers can be stored to increase performance. Using multiple frame buffers allows for queuing multiple pages of data. This can be beneficial for rendering speeds.

The MIPI DSI video mode will be used to send external RAM continuously to the display. This will increase the required MPU frequency to retrieve and send display data to and from RAM. Processor memory is not sacrificed when implementing an external memory to store the frame buffer.

An external memory that is interfaced with the host processor can have timing constraints in maintaining the speeds required to read and write the frame buffer. The frame buffer is stored in RAM and not FLASH because it requires a continuous update. The desired bitmaps or fonts (general display data) are stored in FLASH memory to be sent to RAM for the next display update.

When selecting external RAM for display memory, considerations should be made toward power consumption and performance. SRAM provides the fastest access to the framebuffer to avoid timing issues such as flickering or tearing on the display.

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(2) monitor failures and their consequences, and

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